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09/720,720	02/28/2001	Richard Spitz	10191/1614	3872

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EXAMINER

TRAN, BINH X

ART UNIT	PAPER NUMBER
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1765

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/720,720
Filing Date: February 28, 2001
Appellant(s): SPITZ ET AL.

MAILED

FEB 11 2005

GROUP 1700

Richard L. Mayer
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9-5-2003.

(1) *Real Party in Interest*

Art Unit: 1765

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is correct.

(7) *Grouping of Claims*

The rejection of claims 31 and 35 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) *Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) *Prior Art of Record*

Art Unit: 1765

6,077,451	Takenaka et al.	6-2000
6,432,838	Choi et al.	4-2002
6,136,137	Farnworth et al.	10-2000

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 31, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6,211,010) in view of Takenaka et al. (US 6,077,451) and further in view of Choi (US 6,432,838).

Lee discloses a method for etching comprising the steps of:

selectively etching the silicon element (i.e. polysilicon) with a gaseous etching medium comprising ClF_3 (aka chlorine trifluoride) (step 404 of Fig 4 and col. 5 lines 62-65; Fig 5);

exposing, subsequent to the selective etching, the silicon element to a heat treatment in a vacuum at an elevated temperature (Step 407, Fig 4; Fig 5).

Lee fails to disclose that the etching step forming a gaseous reactive by products. However, Lee clearly discloses the step of etching the same material with applicant using the same etchant (i.e., etching silicon using ClF_3). In a method for etching silicon material, Takenaka discloses that the silicon element is etched with ClF_3 will produce a gaseous reactive products (col. 3 lines 60-67, more specific, equation 3). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify by forming a gaseous by product because it is easy to remove this gaseous by product by pumping it out of the chamber.

Lee also fails to disclose the step of exposing the silicon element to a first heat treatment in a vacuum at a first elevated temperature. In a silicon etching method using ClF_3 , Choi discloses the step of heating the silicon element in a vacuum before the step of etching using ClF_3 to control the etch rate (col. 5 lines 25-33). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Lee/Takenaka in view of Choi by heating the silicon element to the first elevated temperature because it will help to control the etch rate.

Respect to claim 33, both Lee and Choi disclose that the heat treatment is accomplished in a vacuum lock chamber.

2. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, Takenaka, Choi in view of Farnworth (US 6,136,137).

Respect to claim 35, Takenaka discloses that the selective etching step remove (or eliminate) the contaminant (read on impurity) of the polysilicon layer (read on crystal lattice of the silicon) (col. 5 lines 45-50). However, Takenaka does not disclose that the silicon surface is sawn-out part of a silicon wafer. In a semiconductor method, Farnworth teaches the substrate surface can be a sawn-out part of the silicon wafer (Fig 2, col. 4 lines 58-67). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Lee, Takenaka and Choi in view of Farnworth by using a silicon surface that is sawn-out part of a silicon wafer because equivalent and substitution of one for the other would produce an expected result. Further the use of sawn-out part of a silicon wafer is well known in the semiconductor art.

(11) Response to Argument

The appellants argue that the examiner interpretation of the pressure in figure 5 of Lee lead to illogical result. The examiner strongly disagrees. First the appellant point out that the Lee pressure range of 10^{-3} - 10^{-4} Torr during in-situ cleaning (i.e. etching process) is considered as "high" level vacuum. This argument is not commensurate with the scope of the claim. There is no limitation in the claim to limit the specific pressure inside the chamber during the etching process.

Second, the appellant point out that that the examiner's interpretation of Fig 5 lead to a conclusion that the pressure is at absolute vacuum (0 Torr). According to appellant, absolute vacuum is impossible to achieve. The examiner strongly disagrees with this argument. The examiner never suggests or implies that Lee teaches the pressure during the heat treatment step is at absolute vacuum (0 torr). The examiner clearly recognizes that it is impossible to achieve absolute vacuum. The examiner interprets the term vacuum means: a space partially exhausted by artificial means (as an air pump), or a degree of rarefaction below atmospheric pressure. In Figure 5, Lee clearly shows that the pressure inside the chamber is reduced after the pre-cleaning step by using an air pump to pump the gas out of the chamber. Lee further shows that the pressure inside the chamber during the heating treatment is less than the pressure during the pre-cleaning step (Note: Lee's pre-cleaning step is equivalent with appellant's etching step) (See Fig 5). Base on this information, the examiner still maintains that Lee teaches the step of "exposing, subsequent to the selective etching, the silicon element to a second heat treatment in a vacuum at a second elevated temperature".

Third, the appellants point out that the examiner's interpretation of Lee's Fig 5 indicates that the pressure "is at absolute vacuum during the vent step, which is simply impossible". Again, examiner strongly disagrees with this argument. The examiner never suggests or implies that Lee discloses the pressure is at absolute vacuum during the vent step. The examiner interprets that the Lee's pressure during the venting step is lower than the pressure during in-situ pre-cleaning step.

Fourth, the appellants argue, "Choi reference does not disclose that the heat processing is carried out in a vacuum". The examiner strongly disagrees. Choi clearly teaches use turbo pump (86) and baking pump (88) to pump the gas out of the chamber. Choi also discloses that the heating step is performed prior to the introduction of ClF_3 . The pressure inside chamber during the heating step must be under vacuum condition because of the baking pump. Choi further teaches the etching step is performed in vacuum chamber having pumps using ClF_3 etchant gas under low pressure (col. 5). The low pressure exists in the chamber due to the flow of ClF_3 etchant in conjunction with the pump being turn on. Prior to the introduction of ClF_3 (i.e. there is no ClF_3 gas in the chamber), the vacuum must exist because of the pump. Therefore, the examiner still maintains that Choi's reference clearly teaches that the heating step is performed under vacuum condition.

For the above reasons, it is believed that the rejections should be sustained.

Art Unit: 1765

Respectfully submitted,

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January 13, 2005

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